



An SEU-Hard Flip-Flop for Antifuse FPGAs

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Abstract

developed for antifuse FPGA application. Design and An SEU-hardened flip-flop has been designed and application issues, testability, test methods, simulation and results are discussed.





Controlling time with logic

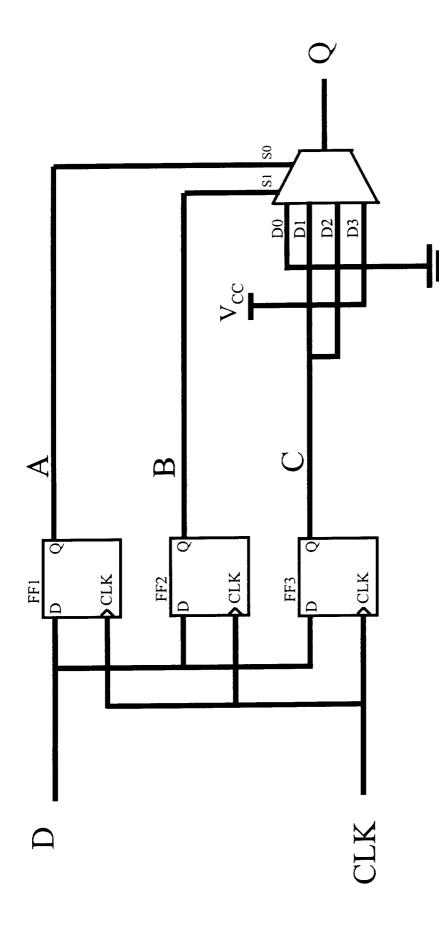


Figure 1. SEU-hardening using available device resources.





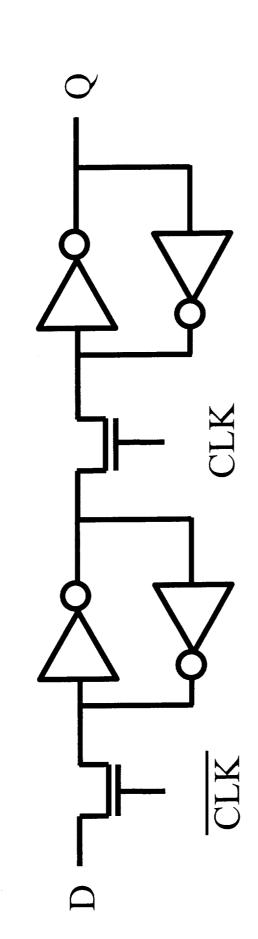
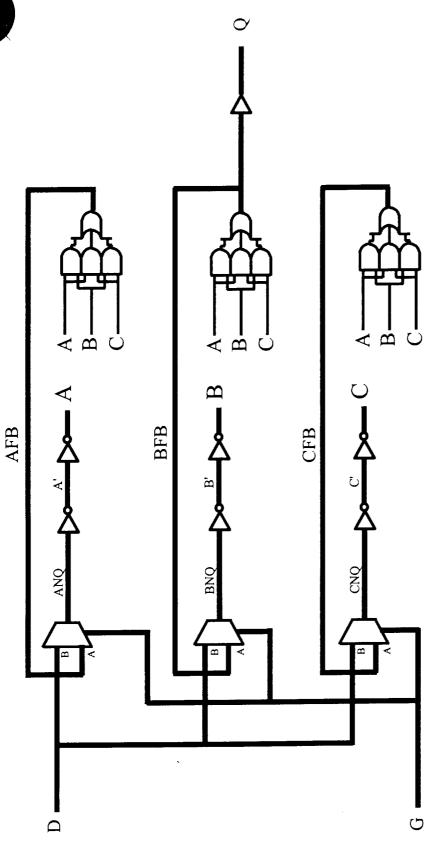


Figure 2. Standard master-slave flip-flop.







asynchronous structure and interlocks eliminate the need Figure 3. K-Latch schematic, simplified. The for a free running clock to scrub SEUs.









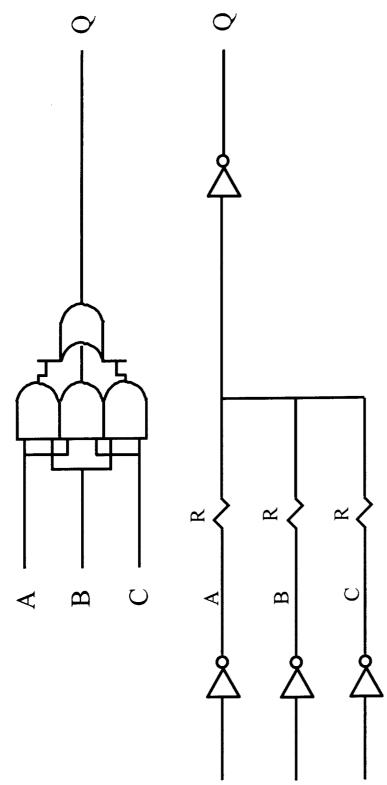


Figure 4. Voter circuit implementations. The top approach glitch-free. The lower half is an application of threshold uses a traditional majority circuit that is designed to be logic principles.







controlling time with logic

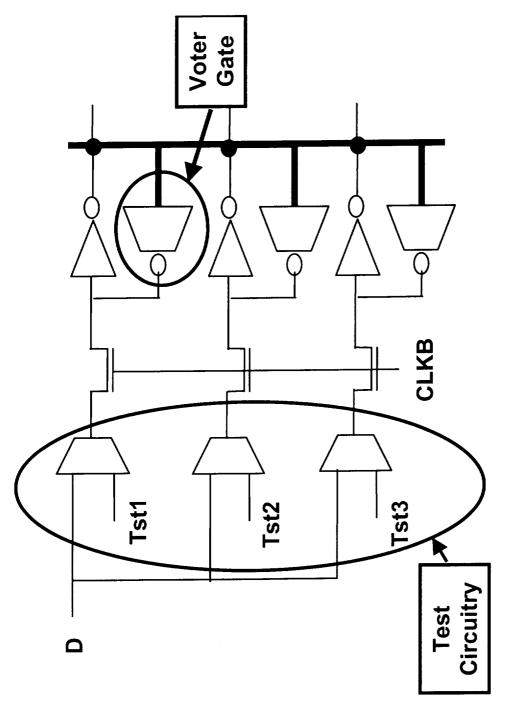
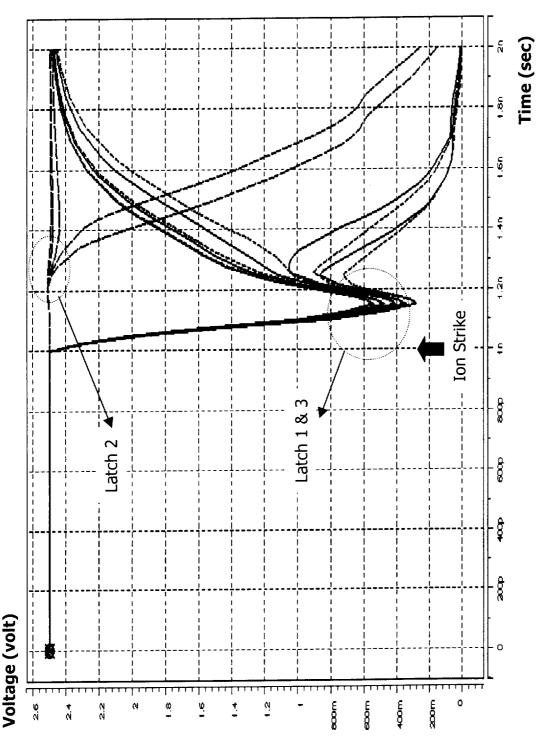


Figure 5. Simplified test circuitry logic.







latches. A heavy ion strikes latch 1 and 3 right at the junctions simultaneously. The collected total charges was used as a parameter to generate a family of curves and to determine the Figure 6. SPICE simulation showing the voltage transient of the sensitive node in the subcritical charge, which is 0.15pC.





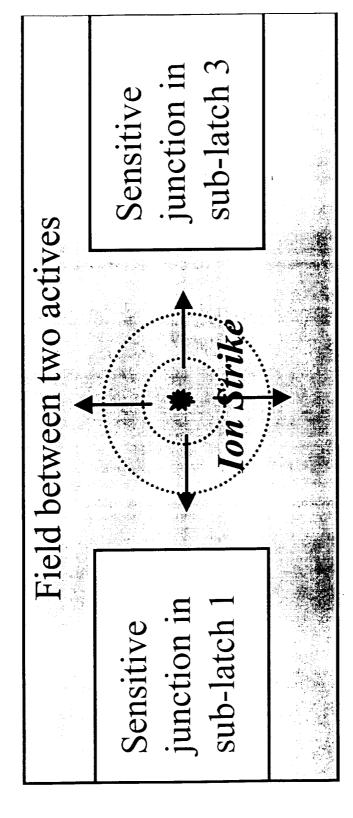
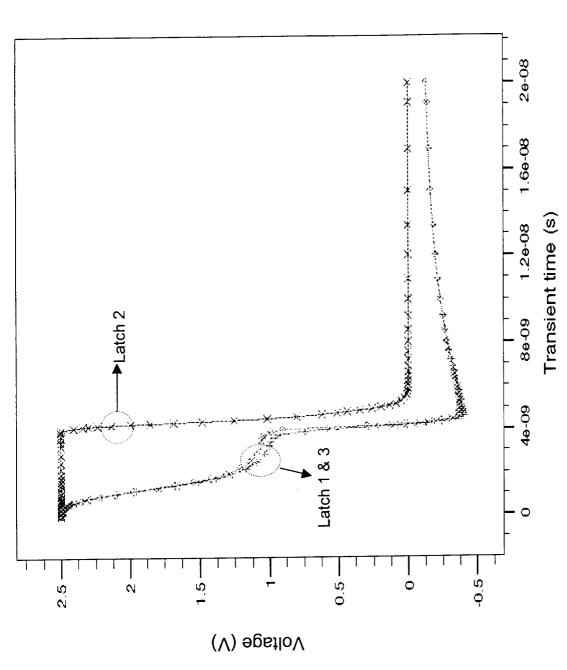


Figure 7. Schematic of 3D mixed-mode simulation, showing a heavy ion strike at the center of the space between the sensitive junction in latch 1 and 3. The induced carriers reach to the junctions by lateral diffusion.





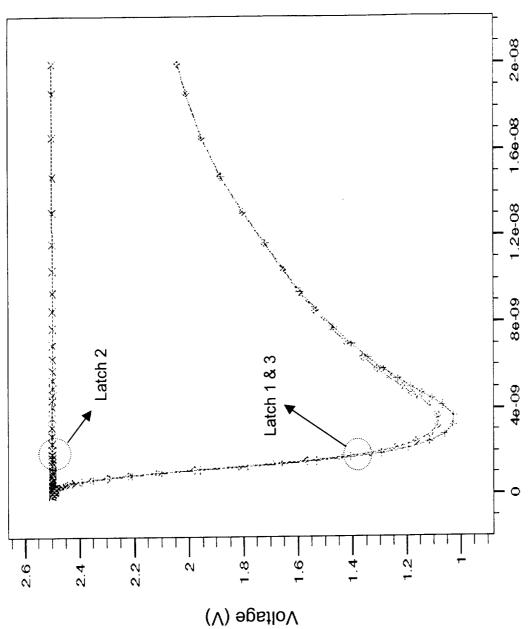


heavy ion with LET=129MeV-cm²/mg stroke at the center of the space (see Figure 7) between the sensitive junctions of latch I and 3. When the voltages in both latch I and 3 reach the logic trip Figure 8. Showing 3D mixed-mode simulation results. Voltage transient of the active node. A point, the triple redundant latch has an upset.





Controlling time with logic



heavy ion with LET=128MeV-cm²/mg stroke at the center of the space (see Figure 7) Figure 9. Showing 3D mixed-mode results. Voltage transient of the active node. A between the sensitive junctions of latch I and 3. The voltages in both latch I and 3 recovered, the triple redundant latch has no upset. Transient time (s)







Test Pattern Description Overview

shift register design is different, to measure different aspects stages, although more then one flip-flop is used for a stage in The primary section of the TMRSX32 pattern consists of 4 of the architecture. The length of each shift register is 100 shift registers, all clocked by a common clock pin. Each two of the designs, in addition to some extra logic.







Test Pattern Description Clocking

buffers intentionally added between flip-flops to increase The CLKBUF and HCLKBUF macros are used to drive the global clock and is available off-chip for external monitoring. No provisions are made to satisfy t_H other than the normal place and route algorithms. That is, there are no delays. There are some buffers added in some shift registers, for example, to measure SETs.







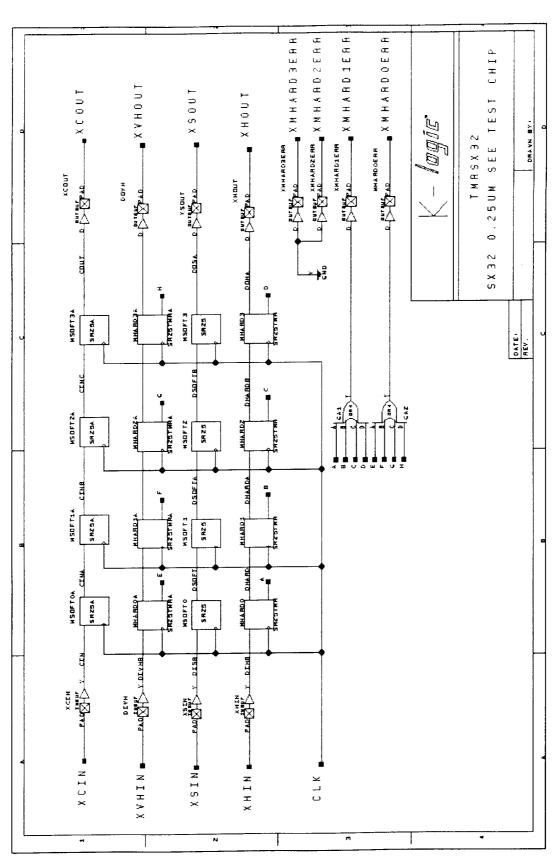


Figure 10. Overview of the logic in the TMRSX32 SEE test chip.







Test Pattern Description MSOFT0A Shift Register



fast signal propagation time of less than 0.1 ns. The output of Direct Connect is a horizontal routing resource that provides SuperCluster. DirectConnect uses a hard-wired signal path requiring no programmable interconnection to achieve its ensure that the Combiner does not eliminate this "unnecessary" logic. Since the BUFF has a fanout of 1, it connections from a C-cell to its neighboring R-cell in a given BUFF has a PRESERVE attribute attached to its output to permits the fastest type of connection, a Direct Connect. The This 100-stage shift register is composed of DF1 R-Cell elements, each of which is separated by a BUFF. this shift register is DOC.





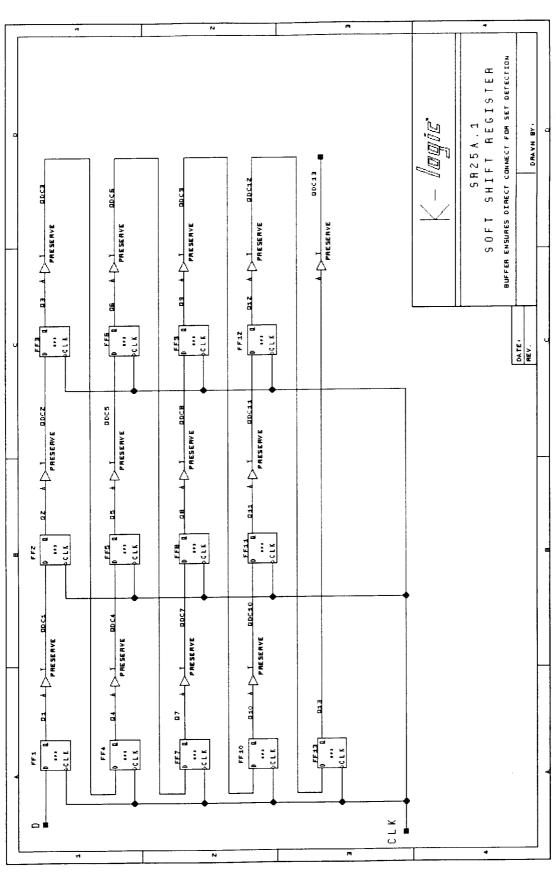


Figure 11. Schematic of a portion of the MSOFT0A shift register. Buffers placed 7/19/2001 between flip-flops aid in the measurement of SET's.





Test Pattern Description MSOFT0 Shift Register



This shift register is identical to the MSOFT0A shift register described above except that there are no BUFFs separating the shift register elements. It is composed of 100 DF1 R-Cell elements.

The output of this shift register is DOS.





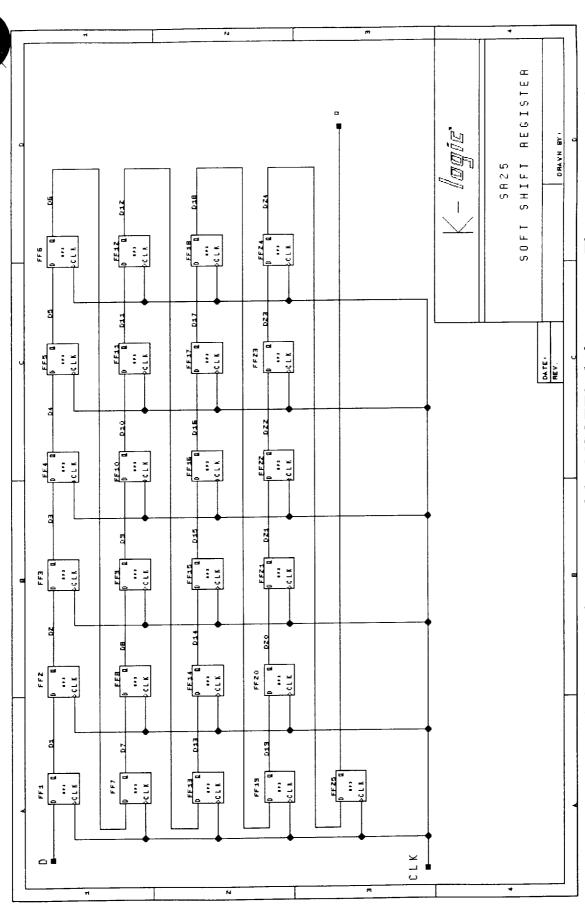


Figure 12. Schematic of a portion of the MSOFTO shift register. This circuit is used to measure the hardness of the K-Latch-based flip-flops, implemented in the S-Cell.



Test Pattern Description MHARD0 Shift Register



majority voting element. The second MX4 and the INV functions as a disagreement detector. The outputs of all This 100-stage shift register is composed of TMR-hardened elements consists of three DFPCB flip-flops and two MX4 [at the user level] flip-flops. Each of these TMR-hardened muxes and an INV inverter. The first mux functions as a disagreement detectors for this register are logically OR'd.

The output of the shift register is DOH. The output of the OR'd disagreement detectors is 1 ERR.





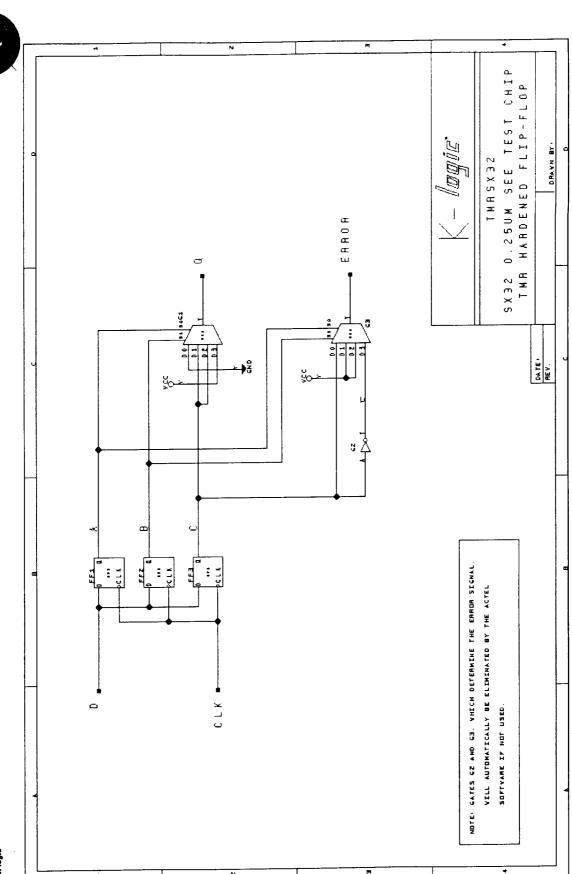


Figure 13. Schematic of a stage in the MHARD0 shift register. Each stage is compose \underline{d} 7/19/2001 of a TMR-triplet, voter, and disagreement detector.



Test Pattern Description MHARD0A Shift Register



The first mux functions as a majority voting element. The second MX4 and the INV functions as a disagreement detector. The outputs of all disagreement flip-flops modified to detect SETs. Each of these TMR-hardened elements This 100-stage shift register is composed of TMR-hardened [at the user level] consists of three DFPCB flip-flops and two MX4 muxes and an INV inverter. detectors for this register are logically OR'd.

CLR* inputs of each of the three DFPCB flip-flops. Similarly, the input of the BUFF is tied to V_{CC} and its output is connected to the three PRE* inputs of the three flip-flops. Any hit on either the INV or the BUFF would be "caught" by the flip-flops. This may result in a combination of logic errors or activation of the disagreement detector, depending on how many of the flip-flops were effected by Each TMR-hardened triplet has been modified by the use of additional BUFF and INV elements. The INV's input is grounded and the output is connected to the

The output of the shift register is DOVH. The output of the OR'd disagreement detectors is 0 ERR.







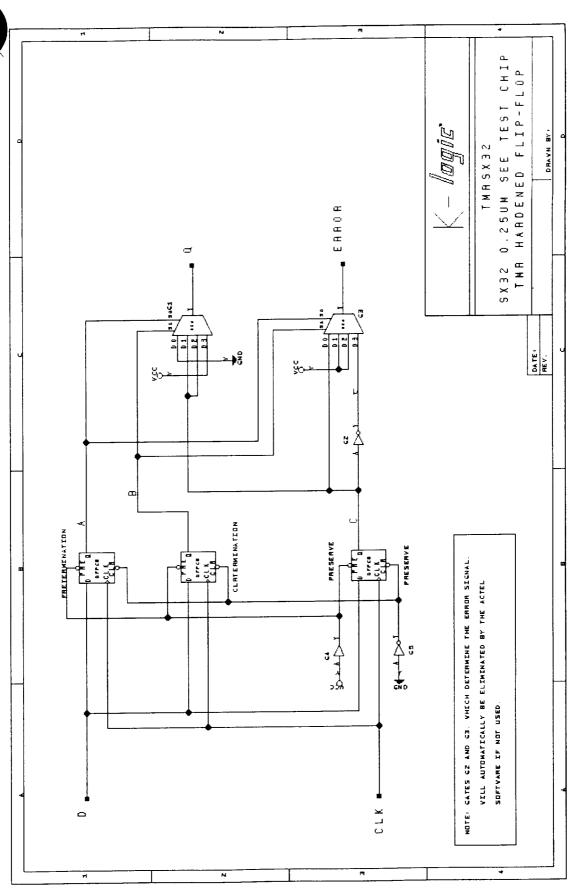
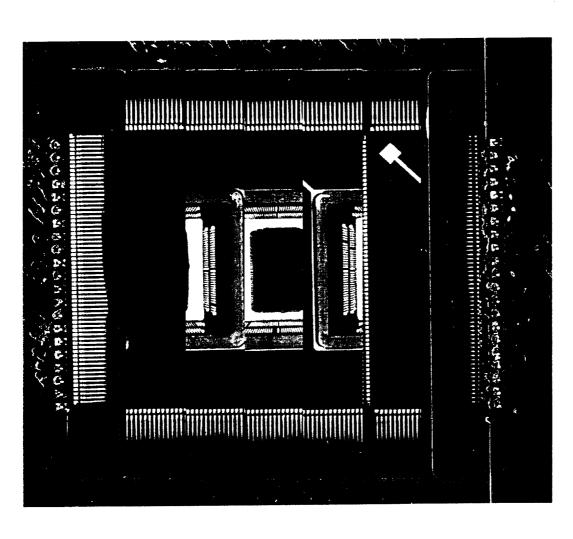


Figure 14. Schematic of a stage in the MHARD0A shift register. The buffer and inverter driving PRE and CLR are used to detect SETs.

The Figure

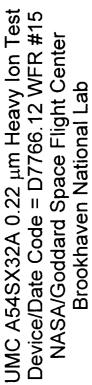


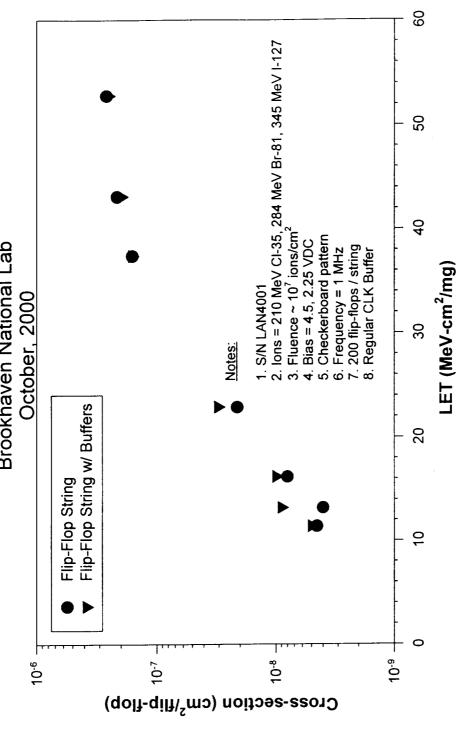


"reverse" mounting of the die, slightly limiting beam angles. Figure 15. DUT mounting. The use of a socket requires









A54SX32-A. Few SEUs were detected for the hardened Figure 16. Cross section-LET curve for a commercial device at an LET \geq 60 MeV-cm²/mg.

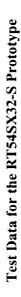












3421 C1 22.9 60, 0 45,225 218 46x10 ⁴ 10 ⁷ 0 0 3421 C1 22.9 60, 90 45,225 217 46x10 ⁴ 10 ⁷ 0	UT S/N	Ion	LET MeV- cm²/mg	Tilt, Roll (degrees)	Supply Voltages	Time (sec)	Flux (p/cm²/s)	Fluence (p/cm ²)	1_Err	рос	SOG HVOG	soa	рон	0_ERR
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169.130, 45 $4.5,2.25$ 314 $3.2x10^4$ 10^7 0159.90, -60 $5.5,3.0$ 302 $3.3x10^4$ $9.9x10^6$ 01104.4 $55,89$ $5.5,3.0$ 608 $1.6x10^4$ 10^7 0			104.4	55, 45	4.5,2.25	339	3.0×10^4	10,	0	0	0	0	0	0
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1 104.4 55,-89 5.5,3.0 608 1.6x10 ⁴ 10 ⁷ 0	ا _, ا	-	59.9	0, -60	5.5, 3.0	302	3.3×10^4	9.9x10 ⁶	0	0	0	0	0	0
		_	104.4	55,-89	5.5, 3.0	809	1.6x10 ⁴	10,	0	0	0	0	0	0







Conclusion

Additionally, single event It is both feasible and practical to design and produce an SEUprocess. As a result, this logic can be used reliably in the radiation environment at costs far less then devices produced on transients in this high-speed, small feature sized process do not appear to be significant. The overhead of the redundant hardened antifuse-based FPGA on a 0.25 µm commercial elements and the correction circuitry has at most only a small a radiation-hardened process. impact on system performance.



